

## WAFER FAB PROCESS TECHNOLOGY

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The Ecole des Mines de St Etienne – site Georges CHARPAK offers a 5-day course entitled «**Wafer Fab Process Technology**». This course provides a comprehensive examination of current silicon wafer Fab technology, from **Crystal growth**, through **Device Formation & Device Interconnect**, to **Parametric Test**. It will also discuss leading-edge process techniques such as cluster beam ion implantation, ALD, SOI technologies, flash RTP annealing, metal gates, strained silicon & more.

### Who Should Attend

This course is designed for semiconductor industry professionals who wish to enhance or update their wafer fab process knowledge. These include process engineers and technologists, process analysts, process integration engineers, yield engineers, equipment engineers, materials scientists, and technical managers.

### Course Notes

A very comprehensive, highly readable course manual is provided.

### Instructor

Jim A. Fraser has 22 years experience in wafer fab process engineering at Nortel Networks and STMicroelectronics. He teaches Microelectronic Manufacturing Processes at the University of Ottawa as a part-time professor, and Wafer Fab Process Technology on contract to the semiconductor industry.

### Fees

3500 € for the 5-day course

### Course Description

Learn the why and the how of all individual wafer fab process techniques, including

- Thermal Processing
- Ion Implantation
- Surface Preparation
- CVD (Chemical Vapour Deposition)
- Epitaxy
- PVD (Physical Vapour Deposition)
- Lithography
- Etch
- CMP (Chemical Mechanical Planarization)

A baseline CMOS process flow will provide a clear introduction to process integration principles and the context for discussion of the individual process techniques.

The rapid and continuous scaling of devices, from the 0.25  $\mu\text{m}$  technology node of ten years ago to today's 45 nm processes, has necessitated evolutionary and revolutionary changes to fab equipment, processes integration, and process techniques. This course will discuss leading-edge process techniques, such as

- continuous Czochralski silicon growth
- cluster beam ion implantation
- flash RTP annealing
- high density plasma etching
- dual-Damascene Cu interconnect
- low-k inter-metal dielectrics
- plasma nitrided oxides
- high-k gate and capacitor dielectrics
- ALD (atomic layer deposition)
- SOI (silicon on insulator) technology
- immersion lithography
- metal gates
- strained silicon

